REMARKS

The above amendments and these remarks are responsive to the Office Action issued on July 20, 2006. By this response, claims 1 and 9 are amended. No new matter is added. A petition for a three-month extension of time is submitted concurrently herewith.

The Office Action

The Office Action dated July 20, 2006 allowed claims 10 and 19, but rejected claims 1, 2, 4, 5 and 7-9 under 35 U.S.C. §103(a) as being unpatentable over Okado (EP 0511484A2) in view of Hennessy (Computer Architecture) and Dean (5,544,342). Claim 6 was objected to for depending from a rejected base claim.

It is respectfully submitted that the rejection is overcome and the objection is addressed in view of the amendments and/or remarks presented herein.

The Obviousness Rejection Based on Okado, Hennessy and Dean Is Traversed

Claims 1, 2, 4, 5 and 7-9 were rejected as being unpatentable over Okado in view of Hennessy. By this Response, independent claims 1 and 9 are amended. It is respectfully submit that the obviousness rejection is overcome because Okado, Hennessy and Dean cannot support a prima facie case of obviousness.

Claim 1, as amended, describes a data processing apparatus comprising an instruction memory in which an instruction is stored, a data memory in which data is stored, and an instruction decoder decoding a fetched instruction. The instruction memory includes a plurality of instruction memory banks. The apparatus further includes a memory operation unit that is coupled to the instruction memory, the data memory and the instruction decoder. The memory operation unit fetches an instruction stored in the instruction memory, and accesses the data

memory according to a decode result of the instruction decoder. An integer operation unit is provided to carry out an integer operation according to a decode result of the instruction decoder. The memory operation unit generates (1) a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle, and (2) a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks. The instruction memory includes a high speed instruction memory, such as cache memory. The memory operation unit generates a pipeline cycle corresponding to instruction readout to carry out a pipeline process when fetching an instruction from the high speed instruction memory. In other words, the number of pipeline stages is rendered variable. Furthermore, the memory operation unit performs a pipeline control having a same throughout and a different latency compared to the access to said instruction memory when accessing to said high speed instruction memory.

It is respectfully submitted that Okado, Hennessy and Dean, either combined or alone, do not reveal that the memory operation unit performs a pipeline control having a same throughout and a different latency compared to the access to said instruction memory when accessing to said high speed instruction memory, as described in claim 1. Since Okado, Hennessy and Dean, even if combined, do not disclose every limitation of claim 1, the cited documents cannot support a prima facie case of obviousness. The obviousness rejection is untenable and should be withdrawn. Favorable reconsideration of claim 1 is respectfully requested.

Claims 2 and 4, 5, 7 and 8, directly or indirectly, depend on claim 1, respectively, and incorporate every limitation thereof. Therefore, the obviousness rejection of claims 2 and 4, 5, 7

and 8, based on Okado, Hennessy and Dean also is untenable and should be withdrawn based on at least the same reasons for claim 1, as well as based on their own merits. Favorable reconsideration of claims 2 and 4, 5, 7 and 8 is respectfully requested.

By this Response, claim 9 is rewritten into independent form and describes a data processing apparatus comprising an instruction memory, a data memory, an instruction decoder decoding a fetched instruction, and a memory operation unit configured to fetch an instruction stored in the instruction memory, and access the data memory according to a decoded result of the instruction decoder. An integer operation unit is provided to carry out an integer operation according to a decoded result of the instruction decoder. The instruction memory includes a plurality of instruction memory banks. The memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle and a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks to carry out a low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks. The memory operation unit reads out data from the data memory via a data input bus, and writes data into the data memory via a data output bus differing from the data input bus. Therefore, an exemplary data processing apparatus according to claim 10 defines two separate buses: a data input bus and a data output bus different from the data input bus, coupled between the memory operation unit and the data memory. In addition, said data memory and said integer operation unit are connected to said data input bus and said data output bus so as to perform an access to said data memory at a high speed.

It is respectfully submitted that Okado, Hennessy and Dean, either combined or alone, do not reveal that said data memory and said integer operation unit are connected to said data input

bus and said data output bus so as to perform an access to said data memory at high speed, as described in claim 9. Since Okado, Hennessy and Dean, even if combined, do not disclose every limitation of claim 9, the cited documents cannot support a prima facie case of obviousness. The obviousness rejection is untenable and should be withdrawn. Favorable reconsideration of claim 9 is respectfully requested.

The Objection to Claim 6 Is Addressed

Claim 6 indirectly depends on claim 1 and was objected to for depending from a rejected base claim. However, as discussed earlier, claim 1 is now in condition for allowance. Therefore, claim 6 is also in condition for allowance by virtue of its dependency.

Conclusion

For the reasons given above, Applicants believe that this application is conditioned for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representatives listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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